In the Claims:

This listing of claims replaces all prior versions.

1. (Previously presented) A system comprising:

a processor that executes logical or arithmetic operations;

a plurality of register bank blocks used as special function registers by the processor during the execution of the logical or arithmetic operations and,

a register bank block decoder circuit for activating one and only one of the plurality of register bank blocks, the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks.

2. (Previously presented) A system according to claim 1, further comprising:

a memory circuit for storing of a first program stream and for storing of a second program stream, wherein the processor utilizes a first register bank block from the plurality of register bank blocks during execution of the first program stream, and upon the occurrence of an interrupt resulting from an interrupt event associated with the second program stream, the processor executes the second program stream utilizing a second register bank block, the second register bank block different and logically isolated from the first register bank block.

3. (Original) A system according to claim 2, wherein the second program stream has a higher interrupt priority than the first program stream.

4. (Previously presented) A system according to claim 1, further comprising:

an input data bus and,

an input switching circuit coupled to the plurality of register bank blocks and having a selection input port for receiving a register bank block selection signal from the register bank block decoder circuit, the input switching circuit for activating one of the plurality of register bank blocks in dependence upon the register bank block selection